

CFG Orion

***Technical Reference Manual***

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**Intel Confidential**

CFG Orion Technical Reference Manual

About This Document

This document is written for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) using Orion NoC IP.

Audience

This document is intended for users of NocStudio:

* NoC Architects
* NoC Designers
* SoC Architects

Prerequisite

Before proceeding, you should generally understand:

* Basics of Network on Chip technology
* AMBA interconnect standards

Related Documents

The following documents can be used as a reference to this document.

* CFG NocStudio Orion User Manual
* CFG Orion IP Integration Spec

Customer Support

For technical support about this product and general information, contact CFG Support.

Revision History

|  |  |  |
| --- | --- | --- |
| Revision | Date | Updates |
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# Introduction

## CFG Orion Overview

CFG Orion is a physically aware, high-performance Network-on-chip (NoC) IP that is used for rapidly designing and analyzing highly efficient and scalable interconnects for a wide variety of SoCs. To quickly produce efficient, high-performance NoC IPs, Orion uses a requirements-driven design approach. Orion uses number of state-of-the-art algorithms to provide robust end-to-end QoS and application-level deadlock avoidance. The solution can scale from low- to medium-end SoCs with 10s of IP blocks to high-end SoCs with 100s of IP blocks and provides bandwidth scaling, optimal latency and clock frequencies of up to 3 GHz. Orion is built upon following the following fundamental design principles.

### Requirements driven approach

Orion is configured and optimized using NocStudio - a NoC architecture exploration platform and interconnect synthesizer. NocStudio enables architects to design, configure and simulate CFG’s NoC IP as well as evaluate multiple SoC architectures. The interconnect can be designed and customized based on system requirements such as bandwidth, latency, traffic profiles, as well as fine-grained requirements such as total and per-flow system bandwidth and chip layout.

### Physically aware latency optimized design

Orion design is physically aware of the layout of the on-chip system components producing an interconnect topology that is customized for the SoC layout. Being physically aware ensures that wiring congestions does not occur late in the design cycle and appropriate number of buffers and pipeline stages are present at various fabric channels to enable smooth backend design. Latency sensitive traffic can use dedicated connections to reduce arbitration and congestions, and 16 levels of QoS are supported for fine-grained bandwidth allocation and prioritization. Based on the system traffic specification and SoC physical layout, NoC topology, fabric components, and their placements are automatically computed using machine-learning and graph theory algorithms to optimize the design for area and power.

## Configurability Options

CFG Orion provides user configurability and flexibility across multiple design dimensions. In addition to providing flexibility of number of ports, interface widths, layout portioning, power and voltage partitioning, etc., significant configurability is also provided to the architect in defining the NoC topology as well as other system level characteristics. Orion supports the following industry standard protocols - AXI4, AXI3, AXI-lite, ACE-lite, AHB and APB – along with many proprietary protocols.